

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 1-42 and 64, and add new claims 43-67 as follows:

Listing of Claims:

1-42. (Cancelled)

43. (New) A discharge circuit for discharging a positive voltage on a p-well drive and an array source of a flash memory cell, the discharge circuit coupled to the p-well drive and the array source receiving first and second discharge signals, the discharge circuit operable in a first mode in response to the first discharge signal to couple the p-well drive and the array source and to discharge the p-well drive and the array source to a first voltage level, and operable in a second mode in response to the second discharge signal to discharge the p-well drive and the array source to a second voltage level.

44. (New) The discharge circuit of claim 43 further comprising an NMOS shorting transistor coupled between the p-well drive and the array source, wherein the p-well drive and the array source junction is prevented from becoming forward biased by turning on the NMOS shorting transistor.

45. (New) The discharge circuit of claim 43 further comprising a first NMOS transistor coupled in series with a first diode-coupled NMOS transistor between the array source and ground.

46. (New) The discharge circuit of claim 43 further comprising a first bypass discharge transistor coupled in parallel with the first diode-coupled NMOS transistor.

47. (New) The discharge circuit of claim 43 wherein the array source is discharged through the first NMOS transistor and the first diode-coupled NMOS transistor at a controlled rate during the first mode.

48. (New) The discharge circuit of claim 43 wherein the array source is discharged through the first NMOS transistor and the first bypass discharge transistor at an uncontrolled rate during the second mode.

49. (New) The discharge circuit of claim 43 further comprising a second NMOS transistor coupled in series with a second diode-coupled NMOS transistor between the p-well drive and ground.

50. (New) The discharge circuit of claim 43 further comprising a second bypass discharge transistor coupled in parallel with the second diode-coupled NMOS transistor.

51. (New) The discharge circuit of claim 43 wherein the p-well drive is discharged through the second NMOS transistor and the second diode-coupled NMOS transistor at a controlled rate during the first mode.

52. (New) The discharge circuit of claim 43 wherein the p-well drive is discharged through the second NMOS transistor and the second bypass discharge transistor at an uncontrolled rate during the second mode.

53. (New) The discharge circuit of claim 43 wherein the p-well drive and the array source are discharged to a voltage level equivalent to an n-channel threshold voltage in the first mode, and wherein the p-well drive and the array source are discharged substantially to ground in the second mode.

54. (New) The discharge circuit of claim 43 wherein the first discharge signal goes active to initiate the first mode and couple the p-well drive to the array source, and the first discharge signal remains active during the second mode.

55. (New) The discharge circuit of claim 43 further coupled to a gate of the flash memory cell and operable in response to the first discharge signal to couple the gate to ground to discharge a negative voltage on the gate.

56. (New) A discharge circuit coupled to the array source and p-well drive of a block of memory cells and receiving first and second discharge signals, the discharge circuit operable in a first mode in response to the first discharge signal to couple the array source to the p-well drive and to discharge the array source and p-well drive until the voltages on the array source and p-well drive are equivalent to a n-channel threshold voltage, the n-channel threshold voltage being substantially less than the initial voltages on the array source and p-well drive, and the discharge circuit operable in a second mode in response to the second discharge signal to discharge the array source and p-well drive substantially to ground.

57. (New) The discharge circuit of claim 56 wherein the p-well drive and the array source are discharged at a controlled rate during the first mode, and wherein the p-well drive and the array source are discharged at an uncontrolled rate during the second mode.

58. (New) The discharge circuit of claim 56 further coupled to the gate of the flash memory cell and operable in response to the first discharge signal to couple the gate to ground to discharge a negative voltage on the gate.

59. (New) A flash memory device, comprising:
an address bus;
a control bus;
a data bus;
an address decoder coupled to the address bus;
a read/write circuit coupled to the data bus;
a control circuit coupled to the control bus;
a flash memory-cell array coupled to the address decoder, control circuit, and read/write circuit, and including an array source and p-well drive; and
a discharge circuit coupled to the array source and p-well drive and coupled to the control circuit to receive first and second discharge signals, the discharge circuit operable in a first mode in response to the first discharge signal to couple the array source to the p-well drive and to discharge voltages on the array source and p-well drive to a first voltage level, and operable in a second mode in response to the second discharge signal to couple the

array source to the p-well drive and to discharge the voltages on the array source and p-well drive to a second voltage level.

60. (New) The flash memory device of claim 59 wherein the p-well drive and the array source are discharged to a voltage level equivalent to an n-channel threshold voltage in the first mode, and wherein the p-well drive and the array source are discharged substantially to ground in the second mode.

61. (New) The discharge circuit of claim 59 wherein the p-well drive and the array source are discharged at a controlled rate during the first mode and at an uncontrolled rate during the second mode.

62. (New) The discharge circuit of claim 59 further coupled to a gate of the flash memory cell and operable in response to the first discharge signal to couple the gate to ground to discharge a negative voltage on the gate.

63. (New) A method for discharging positive voltages on a p-well drive and an array source of a flash memory cell and preventing forward biasing the p-well drive and the array source junction, comprising:

coupling the p-well drive to the array source;
discharging the p-well drive and the array source to a first voltage level; and
discharging the p-well drive and the array source to a second level.

64. (Cancelled)

65. (New) The method of claim 63 further comprising discharging the p-well drive and the array source to the first voltage level at a controlled rate.

66. (New) The method of claim 63 further comprising discharging the p-well drive and the array source to the second voltage level at an uncontrolled rate.

67. (New) The method of claim 63 further comprising discharging a negative voltage on a gate of the flash memory cell to substantially ground.